

**Job Description for Publication:**

Position:	ASIC/FPGA Design Engineer
Job Description:	<ul style="list-style-type: none"><li>● VLSI design engineer that will join Ceragon Digital Solution group</li><li>● Taking part in the architecture and implementation of complex: Wireless Networking IPs, physical layer (PHY) transceiver channels, modem blocks, I.P. integration</li><li>● Working closely with Ceragon design team developing together the next generation ASIC/FPGA</li><li>● Working closely with Ceragon verification team.</li></ul>
Job Requirements:	<p>The ideal candidate has the following:</p> <p>Must:</p> <ul style="list-style-type: none"><li>● BSc in Computer science/ Electrical engineering</li><li>● AT least 3-5 years of experience as <b>VLSI Design Engineer with Verilog</b></li><li>● Background in Networking IPs and SOC architecture (Ethernet, networking processor, CPU etc)</li></ul> <p>Advantage:</p> <ul style="list-style-type: none"><li>● Strong background in signal processing and/or communications protocols-Advantage. (Eth/Pcie/USB etc)</li><li>● Experience with RISC/DSP/CPU processors.</li><li>● Experience with synthesis and STA and SDC (Static Timing Analysis).</li><li>● Experienced in implementation of complex communication IP. (CPU/DSP/Mctrl)</li><li>● understanding of fix point implementation, modulation, coding, detection, equalization, timing/phase recovery.</li></ul> <p><b><u>Tools/Languages:</u></b></p> <p>Verilog VHDL, Code Linter, CDC (Cross Domain Clocking), SDC (Synthesis Design Constraint), Altera/Xilinx, Synthesis, STA (Static Timing Analysis), Specman Verification</p> <p>We are looking for candidates capable of self-learning and working in a dynamic environment, with excellent communication skills and team player, capable of grasping an overall view of complex systems.</p>
Other information	For more clarifications contact <a href="mailto:florentinaa@ceragon.com">florentinaa@ceragon.com</a>
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