Job Description for Publication:

Position:	ASIC/FPGA Design Engineer
Job Description:	• VLSI design engineer that will join Ceragon Digital Solution group • Taking part in the architecture and implementation of complex: Wireless Networking IPs, physical layer (PHY) transceiver channels, modem blocks, I.P. integration • Working closely with Ceragon design team developing together the next generation ASIC/FPGA • Working closely with Ceragon verification team.
Job Requirements:	The ideal candidate has the following: Must: • BSc in Computer science/ Electrical engineering • AT least 3-5 years of experience as **VLSI Design Engineer** with **Verilog** • Background in Networking IPs and SOC architecture (Ethernet, networking processor, CPU etc) Advantage: • Strong background in signal processing and/or communications protocols-Advantage. (Eth/Pcie/USB etc) • Experience with RISC/DSP/CPU processors. • Experience with synthesis and STA and SDC (Static Timing Analysis. • Experienced in implementation of complex communication IP. (CPU/DSP/Mctrl) • understanding of fix point implementation, modulation, coding, detection, equalization, timing/phase recovery. **Tools/Languages:** Verilog VHDL, Code Linter, CDC (Cross Domain Clocking), SDC (Synthesis Design Constraint), Altera/Xilinx, Synthesis, STA (Static Timing Analysis), Specman Verification We are looking for candidates capable of self-learning and working in a dynamic environment, with excellent communication skills and team player, capable of grasping an overall view of complex systems.
Other information	For more clarifications contact florentinaa@ceragon.com
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